In re Application of:
Luciano Zoso et al.
Serial No.: 10/730,174
Filed: December 8, 2003
For: HARDWARE FOR PERFORMING AN ARITHMETIC FUNCTION

December 19, 2007

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Certificate of Submission

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December 19, 2007
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Printed Name of Person Signing Certificate

APPEAL BRIEF

COMMISSIONER FOR PATENTS
ALEXANDRIA, VA 22313
BOARD OF PATENT APPEALS & INTERFERENCES:

This brief is filed in the matter of the Appeal to the Board of Appeals and Interferences of the rejection of the claims of the above-referenced application for patent.

REAL PARTY IN INTEREST

The present application is wholly assigned to FREESCALE SEMICONDUCTOR, INC., with its headquarters in Austin Texas.

RELATED APPEALS AND INTERFERENCES

Appellants are unaware of other appeals or interferences which will directly affect, be directly affected by, or have a bearing on the Board's decision in this appeal.

STATUS OF CLAIMS

Claims 6-18 and 20-22 are pending. Claims 1-5 have been withdrawn.

Claims 6-18 and 20-22 stand rejected under 35 U.S.C. 101 as being directed to non-statutory subject matter.

The rejection of claims 16-18 and 20-22. The rejection of claims 6-15 is being appealed.

STATUS OF AMENDMENTS

An amendment received by the U.S.P.T.O. on May 29, 2007, was filed in response to a rejection, was entered, and accurately reflects the pending claims. A final rejection was made on July 11, 2007. A response to the final rejection was received by the U.S.P.T.O. on August 30, 2007. An advisory action was provided on September 7, 2007, sustaining the final rejection. A pre-appeal brief review was requested on September 26, 2007. An action sustaining the final rejection was provided November 15, 2007.

SUMMARY OF CLAIMED SUBJECT MATTER

A hardware solution is provided for performing an arithmetic function and is particularly relevant to for division and taking a square root. The particular technique is implemented in separate circuit blocks without requiring a multiplier. By having separate circuit blocks for performing the arithmetic function a CPU is not required also.

Independent claim 16 is an apparatus claim directed to a circuit that performs an arithmetic function and provides a result of the arithmetic function.

Claim 16 recites a counter supported by counter 12 in FIGs. 1 and 2. The counter provides a count that identifies a current partial iteration. As described at page 5, lines 6-9, the counter is initially set to the resolution of the system minus 1, which in the described example is 15 because the resolution of the system is 16 bits. As described at page 6, lines 12-15, the counter is decremented with each iteration and indicates which bit is being calculated in the current iteration.

Claim 16 further recites a comparator that is supported by comparator 26 of FIGs. 1 and 2 that receives the number on which the arithmetic function is being performed. As described at page 5, lines 23-26, and page 6, lines 1-7, the comparator compares the number to a result based on the current iteration and provides an output indicative of the result of the comparison.

Claim 16 further recites a register means supported by register 14 in FIGs. 1 and 2. The register means has a first input coupled to the output of the comparator. This is shown in FIGs. 1 and 2 and described at page 4, lines 17 and 18. The register means stores a current estimate of the result, provides an output representative of the next iteration, and updates the result based on the output of the comparator. This is described along with describing the function of the comparator and comparator at page 6, lines 7-11; page 6, lines 9-11 and 13-20; page 7, lines 15-26; page 8, lines 1-4;

Claim 16 further recites a storage means supported by register 30 shown in FIGs. 1 and 2. The storage means stores an inverse of the arithmetic function of the current estimate and provides it on an output. This is described at page 5, lines 24-26, and page 6, lines 1-11. The current iteration may be unchanged due to the outcome of the comparison so that the output of register 30 is fed back through mux 28 to its input or it may be updated by the sum of the output of register 30 and programmable shifter 22 through mux 28. This describes providing an output as the output of shifter 22 that has an incremental effect added to the inverse of the mathematical function which in the case of the square root is squaring. Thus, what is provided is that which when added to the output of the storage means is the square of the sum of the current estimate and the next partial iteration. The operation of shifter 22 for the division case is described at page 8, line 26, and page 9, lines 1-6 and 18-24. Because multiplication is the inverse function of division, the affect is that the sum of output of shifter 22 added to the output of register 30 is the same as the divisor multiplied by the next iteration.

Claim 16 further recites summing means which is supported by summer 24 of FIGs. 1 and 2. This sums the output of the storage means and the incremental means which are supported by the outputs of register 30 and programmable shifter 22. The summing means provides the result of the sum to the second input of the comparator.

The operation of summer 24 is described at page 5, lines 24-26; page 6, lines 1-7 and 23-26; page 7, lines 1-3; page 8, lines 15-17; and page 9, lines 5-12 and 21-25.

Dependent claim 17 identifies the arithmetic function as division using a divisor and is supported by FIG. 2.

Dependent claim 18, which depends on claim 17 and is thus relevant to the division embodiment, further characterizes the incremental means as a programmable shifter which is supported by programmable shifter 22 of FIG. 2.

Dependent claim20, which depends on claim 16, identifies the arithmetic function as square root which is supported by FIG. 1.

Dependent claim 21, which depends on claim 20, further characterizes the incremental means as having four separate circuits. One is a means for providing a signal having a value of two times the current estimate which is supported by shifter 16. This doubling arises from a shift of one to the left which is effectively multiplying by two. Another circuit is a means for generating a signal having a value of an incremental increase which is supported by programmable shifter 18. Shifter 18 is the source of the incremental increase based on counter 12. Another circuit is means for summing two times the current estimate and the incremental increase which is supported by summer 20 which sums the outputs of shifters 16 and 18. Another circuit is means for multiplying the sum of the current estimate and the incremental increase by the incremental increase, which is supported by programmable shifter 22. The amount of the shift of both shifters 18 and 22 is controlled by counter 12 so that the result is that multiplication of the output of summer 20 is by the incremental increase.

Dependent claim 22, which depends on claim 20, further characterizes the incremental means as having four separate circuits similar to claim 21. One circuit element is a first shifter that shifts a one by predetermined amount which is supported by shifter 18 which shifts a one determined by the counter. Another circuit is a second shifter that provides an output of the current estimate by one which is supported by shifter 16. Register 14 provides the current estimate to shifter 16 where it is shifted by one. Another circuit is a summer that sums the outputs of the first and second shifters which is supported by summer 20 as is apparent from FIG. 1. Another circuit is a third shifter that shifts the output of the summer by the predetermined amount which is supported by shifter 22. As is shown in FIG. 1, shifter 22 is coupled to counter 12 as is shifter 18 to be shifted by the same predetermined amount.

GROUNDS FOR REJECTION TO BE REVIEWED ON APPEAL

1. Are claims 16-18 and 20-22 directed to patentable subject matter under 35 U.S.C. 101?

ARGUMENT

Arguments for Ground 1

Independent Claim 16

Independent claim 16 and dependent claims 17, 18, and 20-22 stand rejected under 35 U.S.C. 101.

As pointed out in the application, this is a hardware implementation of performing an arithmetic function, especially square root or division. The purpose of this implementation is to be able to perform the desired function without requiring a microcomputer or a multiplier. Thus, there are claimed separately identifiable circuit elements that perform different functions to achieve the arithmetic function. Some of these are means plus function elements and describe a circuit having a particular function so that the arithmetic function is broken into certain identifiable circuit blocks. Two of the claimed elements in claim 16 are claimed as known hardware elements; a counter and a comparator. Although perhaps not optimum, the particular algorithm for achieving a square root, for example, used by applicants could be carried out by a processing unit or a microcomputer that uses general purpose registers to perform the described shifting, counting, storing, and comparing. In such case, however, there would not be separately identifiable hardware blocks in the manner claimed.

Claim 16 has an incremental means that is supported by either 3 shifters and a summer in the case of square root or a shifter in the case of division. Applicants have found a technique for achieving needed multiplication using shifting techniques rather than a multiplier. Each shift of one bit achieves a multiplication by two. A multiplication by two could be achieved using a multiplier. Of course that would probably be considered a poor choice but it could be done. Dependent claims 17 and 18 together claim a divider that uses a programmable shifter. The programmable shifter could be replaced by a multiplier. The amount to be multiplied could be provided by

something other than a counter. Dependent claims 20 and 21 together claim circuit that takes a square root that includes two means clauses that describe multiplying. Those could be replaced with multipliers instead of what is described in the specification and the equivalents thereof. A multiplier cannot be considered an equivalent because the described intent is to avoid using a multiplier. Similarly, claims 20 and 22 together claim a circuit that takes a square root in which three shifters are included. The second and third shifters in particular could be replaced by a multiplier. Accordingly, applicants see no basis for the Examiner's view that this is situation in which all implementations of an algorithm are precluded.

Applicants also do not see the merit in the Examiner's position of characterizing circuit elements that have inputs and outputs that are coupled together, even if they are characterized as performing a function, as an algorithm. Virtually any circuit element can be characterized mathematically. This includes functional blocks such as amplifiers and filters down to passive circuit elements like resistors and capacitors.

In addition, the CAFC cases AT&T v. Excel Commc'ns, Inc. 172 F.3d 1352 (1999) and the just decided In Re Stephen W. Comiskey 2006-1286 (Serial No.09/461,742) (2007) held that hardware implementation of an algorithm was patentable. In fact the court in In Re Stephen W. Comiskey at page 23 even characterized AT&T as "holding patentable a method for determining whether long distance calls being made between long-distance carriers or within a single long-distance carrier that used a mathematical algorithm and 'require[d] the use of switches and computers.'"

CONCLUSION

For at least the reasons set forth above, Applicants respectfully submit that the claims of the present application are directed to patentable subject matter.

Respectfully submitted,

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Claims Appendix

1. (withdrawn) A circuit for taking the square root of a square value, comprising:

a first register for storing a current estimate having an input and an output;

a first shifter having an input coupled to the output of the first register and an output;

a counter having an output;

a second shifter having an input coupled to the output of the counter and an output, wherein a shift amount is responsive to the output of the counter;

a first summer having a first input coupled to the output of the first shifter, a second input coupled to the output of the second shifter, and an output;

a third shifter having a first input coupled to the output of the summer, a second input coupled to the output of the counter, and an output;

a second summer having a first input coupled to the output of the third shifter, a second input, and an output;

a comparator having a first input coupled to the output of the second summer, a second input for receiving the square value, and an output coupled to the input of the first register;

a multiplexer having a first input coupled to the output of the second summer, a second input coupled to the second input of the second summer, a third input coupled to the output of the comparator; and an output; and

a second register having an input coupled to the output of the multiplexer and an output coupled to the second input of the second summer.

2. (withdrawn) The circuit of claim 1, further comprising a logic circuit having an input for receiving a clock circuit and an output coupled to the counter, the first register, and the second register.

3. (withdrawn) A method of performing an iteration for calculating a square root of a square value, comprising:

providing an estimate of the square root;

performing a left shift of one on the current estimate to form a first shifted output;

shifting a one by a counter amount to form a shifted one output;

adding the shifted one output to the first shifted output to form a first added number;

performing a left shift of the counter amount on the first added number to form a second shifted output;

adding the second shifted output to a square of the current estimate to form a squared estimate;

comparing the squared estimate to the square value to determine a state of an update output;

updating the current estimate and the square of the current estimate based on the update output.

4. (withdrawn) The method of claim 3, wherein the updating comprises changing the square of the current estimate to be equal to the squared estimate if the update output is in a first state and leaving the square of the current estimate unchanged if the update output is in a second state.

5. (withdrawn) In a method of calculating a square root by calculating bits of an estimated square root in descending order of significance in which the uncalculated bits are zero, a method for calculating a next bit comprising:

shifting the estimated square root in the direction of more significance by one to provide a shifted estimated square root;

providing a one at a bit location of a first number corresponding to the next bit to provide an iterative value;

adding the iterative value to the shifted estimated square root to provide a first added value;

shifting in the direction of more significance the added value by the first number to provide a shifted added value;

adding the shifted added value to a square of the estimated square root to provide an estimated squared value;

comparing the estimated squared value to the square value and providing an update output indicative of the comparison; and

applying a one as the next bit in the estimated square root if the update output is in a first state.

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6. (previously presented) A method of performing an arithmetic function to achieve a result based on a number (square) on which the arithmetic function is performed, comprising

storing a first partial iteration of the result in a first register;

performing an inverse of the arithmetic function on the first partial iteration to determine a first estimated inverse;

comparing the first estimated inverse to the number;

if the first estimated inverse is greater than the number, removing the first partial iteration of the result from the first register;

if the first estimated inverse is less than the number, [[:]] storing the first estimated inverse in a second register and leaving the first partial iteration in the first register;

wherein the first register stores a first result with a first resolution, wherein the second register stores an incremental effect of the first result;

storing a ~~first~~ second partial iteration in the first register;

determining an incremental effect of the second partial iteration on the inverse arithmetic;

adding the incremental effect of the second partial iteration to the incremental effect of the first result to provide a second estimated inverse; and

comparing the second estimated inverse to the number;

if the second estimated inverse is greater than the number, removing the first partial iteration of the result from the first register; and

if the second estimated inverse is less than the number, storing the second estimated inverse in the second register and leaving the second partial iteration in the first register;

wherein the first register stores a second result with a second resolution greater than the first resolution, wherein the second register stores an incremental effect of the first result and the second result.

7. (original) The method of claim 6, wherein the arithmetic function is square root.

8. (previously presented) The method of claim 7, wherein the incremental effect of the second partial iteration comprises two times the first estimated inverse times the second partial iteration plus the second partial iteration squared.

9. (previously presented) The method of claim 8, wherein determining the second partial iteration comprises shifting a one by a predetermined amount.

10. (previously appealed) The method of claim 9, wherein determining the incremental effect of the second partial iteration comprises:

determining two times the first estimated inverse by shifting the first estimated inverse by one;

adding the first partial iteration to two times the first estimated inverse to provide a first inverse sum; and

multiplying the first inverse sum by the first partial iteration by shifting the first inverse sum by the predetermined amount.

11. (original) The method of claim 10, wherein the square root is of the number.

12. (original) The method of claim 6, wherein the arithmetic function is division.

13. (currently amended) The method of claim 12, wherein the incremental effect of the second partial iteration comprises one half the first partial iteration times the divisor.

14. (original) The method of claim 13, wherein performing an inverse function on the first iteration comprises shifting the divisor by predetermined amount.

15. (currently amended) The method of claim 14, wherein determining the incremental effect of the second partial iteration comprises shifting the divisor by an amount equal to the predetermined amount minus one.

16. (previously presented) A circuit for performing an arithmetic function applied to a number and provide a result of the arithmetic function based on partial iterations, comprising:

a counter for providing a count to identify a current partial iteration;

a comparator having a first input for receiving the number, a second input, and an output;

register means, having a first input coupled to the output of the comparator, a second input coupled to the counter, and an output, wherein the register means is for storing a current estimate of the result of the arithmetic function as applied to the number based on previous partial iterations, for providing an output representative of a next partial iteration, and for updating the result based on the output of the comparator;

storage means for storing an inverse of the arithmetic function of the current estimate and having an output on which is provided the inverse of the arithmetic function of the current estimate of the result;

incremental means having an input coupled to the output of the register means for providing, on an output, an incremental effect, wherein the incremental effect is a value that when added to the inverse of the mathematical function of the current estimate is equal to the inverse function of a next current estimate plus the next partial iteration; and

summing means, having an output coupled to the second input of the comparator, a first input coupled to the output of the storage means, a second input coupled to the incremental means, for providing on the output a sum of the incremental effect and the inverse of the arithmetic function of the current estimate.

17. (original) The circuit of claim 16, wherein the arithmetic function is division by a divisor.

18. (original) The circuit of claim 17, wherein the incremental means comprises:

- a programmable shifter having a first input for receiving the divisor, a second input for receiving a signal indicating a shift amount, and an output coupled to the summing means.

19. (canceled)

20. (original) The circuit of claim 16, wherein the arithmetic function is square root.

21. (original) The circuit of claim 20, wherein the incremental means comprises:

means for providing a signal having a value of two times the current estimate;

means for generating a signal having a value of an incremental increase equal to the difference between the current estimate and the next estimate;

means for summing two times the current estimate and the incremental increase; and

means for multiplying the sum of the current estimate and the incremental increase by the incremental increase to generate the incremental effect.

22. (original) The circuit of claim 20, wherein the incremental means comprises:

a first shifter for providing an output of a shift of a one by a predetermined amount;

a second shifter for providing an output of a shift of the current estimate by one;

a summer for providing an output of a sum of the outputs of the first and second shifters;

a third shifter for providing an output of a shift of the predetermined amount of the output of the summer to the summing means.

23. (canceled)

Evidence Appendix

No evidence is submitted in this appendix

Related proceedings Appendix

There are no decisions under this appendix.